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| 10/570,236 | 02/28/2006 | Pieter Van Der Wolf | NL031032 | 2510 |

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| EXAMINER | |
|---|---|
| GIARDINO JR, MARK A | |

| ART UNIT | PAPER NUMBER |
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| 2185 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/570,236 | VAN DER WOLF ET AL. | |
| | Examiner | Art Unit | |
| | MARK A. GIARDINO JR | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7,9-13 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-13, and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## ***DETAILED ACTION***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/2/2008 has been entered.

The instant application having Application No. 10/570,236 has a total of 13 claims pending in the application, there is 1 independent claim and 12 dependent claims, all of which are ready for examination by the examiner.

## REJECTIONS BASED ON PRIOR ART

### ***Claim Rejections - 35 USC ' 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9-14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu in view of Foster and Denneau.

**Regarding Claim 1**, Sindhu teaches a data processing system, comprising a memory device (main memory 13) and a plurality of data processors (processors 12) provided for accessing to said memory device wherein a communication interface is

coupled between said memory device and said plurality of data processors, said communication interface including a network of nodes (controllers 21 and busses 15) and a memory interface (interface on controllers 21 to main memory controller 25 and arbiter 36), each node comprising at least one slave port for receiving a memory access request from a data processor or from a previous node (connections from the processor cache 16 to the bus 15) and at least one master port (connection from controller 21 to bus 26) for issuing a memory access request to a next node or to said memory device in accordance with the memory access request received at said slave port, wherein one or more slave ports (slave port of node containing bus 15) are connected to one of said data processors (processors 12), wherein one or more master ports (connection from controller 21 to bus 26) are connected to the memory interface, wherein the memory interface arbitrates access to the memory device (Column 6 Lines 23-38).

However, Sindhu does not teach physical location of the communication interface (comprising controllers 21, busses 15, and arbiter 36) in relation to the global memory (main memory 13), thus it is unknown if the communication interface is positioned on a single chip, wherein the memory device is not positioned on the single chip. Foster (US 6,634,034) teaches a communication interface (arbiter 36 in Foster) on a separate chip than the memory (global memory 26 in Foster, also see Column 5 Lines 37-43 and Figure 2, the memory device is on an entirely separate card). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have positioned the communication interface on a single chip, since many processors do not contain a node (such as controllers 21 in

Sindhu) and adding these controllers on the chip with the arbiter would allow the device to work with a wide range of processors, not just ones with controllers (note in Figure 4B in Foster how the processor node has no controller to access the arbiter; the controlling is done by arbiter 36) . Keeping the memory on a separate chip (contained on the memory cards 26 in Foster) allows for greater flexibility, since one may choose to add cards with less RAM for a less expensive system or cards with more RAM for a higher performance system (Column 5 Lines 6-8 in Foster). So, by combining the devices, additional benefits are obtained.

Also, neither Sindhu nor Foster teaches the ability to selectively access a memory request using an address range within a single address space to distinguish between the local cache and main memory. Denneau et al (US 2003/0028747) teaches using separate address ranges for a cache and a main memory (see Figure 3, where the "area used primarily by P0 and P1" and the separate processor stacks have a different address than the global memory, also see accompanying description on Paragraphs 0039-0040). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used separate address ranges (as in Denneau) for the caches and global memory (in the device of Sindhu), because of the additional flexibility provided (second half of Paragraph 0008 in Denneau).

The combined device teaches all limitations of Claim 2, since Sindhu, Foster, and Denneau teach the data processing system according to claim 1, wherein at each node

the number of said slave ports is higher than the number of said master ports (see Figure 1 in Sindhu, where each node has at least two slave ports and at most one master port).

The combined device teaches all limitations of Claim 3, since Sindhu, Foster, and Denneau teach the data processing system according to claim 2, characterized in that said network of nodes is hierarchically structured (see Figure 1 in Sindhu, where three child nodes connect to one parent node, implying a hierarchy; also discussion of hierarchy on Column 5 Lines 14-19).

The combined device teaches all limitations of Claim 4, Sindhu, Foster, and Denneau teach the data processing system according to claim 3, wherein said network of nodes is arranged in a directed acyclic graph structure (see Figure 1 in Sindhu where the master ports of the node containing controllers 21 are connected to slave port of node containing bus 26; note that bus requests branch from nearest the processor at the cache level to farthest from the processor at main memory, rendering the graph directed, also see description of interconnection on Column 5 Lines 28-45).

The combined device teaches all limitations of Claim 5, since Sindhu, Foster, and Denneau teach the data processing system according to claim 4, wherein said network of nodes is arranged in a tree structure (see Figure 1 in Sindhu, where the child and parent nodes are arranged in a tree structure; also discussion of the tree structure in Column 5 first full paragraph).

The combined device teaches all limitations of Claim 6, since Sindhu, Foster, and Denneau teach the data processing system according to claim 1, and Sindhu further

teaches wherein said network of nodes include n groups of nodes with n >= 2 (see Figure 1, where n = 2), wherein each of the slave ports of the nodes of a first group (nodes containing busses 15) is connected to one of said plurality of data processors (processors containing caches 16), the master ports of the nodes of the $n^{th}$ group (nodes containing controllers 21) are coupled to said memory device (memory means containing controller 25 and main memory 13), and each of the slave ports of the nodes of the nth group is connected to a master port of the nodes of the $(n-1)^{th}$ group (the master port of the nodes containing busses 15 are connected to the slave port of the nodes containing controllers 21).

The combined device teaches all limitations of Claim 7, since Sindhu, Foster, and Denneau teach the data processing system according to claim 1, and Sindhu further teaches wherein said nodes are hubs (nodes containing busses 15 as well as node containing bus 26).

The combined device teaches all limitations of Claim 8, since Sindhu, Foster, and Denneau teach the data processing system according to claim 1, and Sindhu further teaches wherein said communication interface further includes at least one local memory unit adapted to be selectively accessed to by a memory request (RAMs 19).

The combined device teaches all limitations of Claim 9, since Sindhu, Foster, and Denneau teach the data processing system according to claim 1, and Sindhu further teaches wherein at least one node means further comprises at least one memory port to which a local memory unit is connected (see the port connecting RAMs 19 to controllers 21).

The combined device teaches all limitations of Claim 10, since Sindhu, Foster, and Denneau teach a data processing system according to claim 1, and Sindhu further teaches wherein said communication interface includes a cache controller for controlling at least a section of the local memory unit as a cache memory (controller 21, also see Column 4 Lines 51-54).

The combined device teaches all limitations of Claim 11, since Sindhu, Foster, and Denneau teach the data processing system according to claim 1, and Sindhu further teaches wherein said communication interface further includes at least one synchronization means for streaming communication between data processors (arbiters 35 are such a synchronization means, see description of this device in the last paragraph of Column 7).

The combined device teaches all limitations of Claim 12, since Sindhu, Foster, and Denneau teach the data processing means according to claim 11, and Sindhu further teaches wherein at least one node includes said synchronization means for streaming communication between the data processors means directly or indirectly coupled to said nodes (arbiters 35 are indirectly coupled to the node means through caches 16, see Figure 1).

The combined device teaches all limitations of Claim 13, since Sindhu, Foster, and Denneau teach the data processing system according to claim 11, and Sindhu further teaches wherein the local memory unit is configured to provide storage based on a first-in/first-out function (which is well known in the art; see US 2002/0188811 Paragraph 0008) and said synchronization means comprises a first-in/first-out

administration means for controlling said local memory unit (the arbiter uses an algorithm that includes FIFO, see Column 8 Lines 18-24).

The combined device teaches all limitations of Claim 14, since Sindhu, Foster, and Denneau teach the data processing system according to claim 8, and Sindhu further teaches wherein said memory device and said local memory unit have a single address space (the memories are organized as a cache-like hierarchy, Column 5 Lines 20-23, also see the shared write updating, which implies a shared address space on Column 16 Lines 44-52, also see how higher level caches aren't checked if a lower level cache contains the information, and if the lower level cache is missing the information, the higher level memory is checked, and the lower level cache is updated with this information, which also strongly points toward a shared address space, Column 22 Lines 41 to Column 23 Line 27).

The combined device teaches all limitations of Claim 15, since Sindhu, Foster, and Denneau teach the data processing system according to claim 1, and Sindhu further teaches wherein at least a portion of said plurality of data processors means is positioned on said single chip (providing circuitry on a chip is well known in the art).

**RESPONSE TO ARGUMENTS**

In response to applicant's argument that Sindhu and Foster fail to disclose that the global and local memories organized such that an address range defines the particular memory, it has been considered but is moot in view of the new grounds of rejection.

**CLOSING COMMENTS**

***Conclusion***

**STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

**CLAIMS NO LONGER IN THE APPLICATION**

Claims 8 and 14 were cancelled by the amendment dated 3/14/2008.

**CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, claims 1-7, 9-13, and 15 have received a first action on the merits and are subject of a first action non-final.

**DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

July 17, 2008

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185